Design considerations of GaN devices for improving power-converter efficiency and density

Salil Chellappan
Systems Manager,
Power Delivery Industrial Systems
Texas Instruments

The availability of Gallium Nitride (GaN) devices for power conversion is improving, with many manufacturers releasing catalog parts.

The application of these devices has gained the keen attention of power-system designers from all over the world. Although a lot of study has gone into understanding their properties, the selection of GaN devices for various power-conversion applications based on their properties remains not well understood.

After much study dedicated to GaN as an alternative to silicon in power switching, multiple manufacturers now offer GaN switching devices for power-conversion applications. However, you must look at the properties of GaN devices in detail before assessing their suitability and advantages. This white paper will examine some of the most important design considerations affecting power-converter performance.

Device architecture

GaN switching devices come in two different types based on their internal architecture: enhancement mode (e-GaN) and cascoded depletion mode (d-GaN). An e-GaN switch operates like a normal silicon metal-oxide semiconductor field-effect transistor (MOSFET), although it has reduced gate-to- source voltage levels. An e-GaN device also has a simpler architecture and packaging, low on-resistance, and zero body-diode reverse recovery (there is no body diode, but the channel itself is bidirectional in nature and behaves like a body diode).

The first (and main) concern with this type of device is the critical nature of its gate-drive design. The problem is that the device's fully enhanced gate-drive voltage is very close to its breakdown voltage – the safety margin is typically only about 1 V. This might cause a device failure in the event of a voltage spike or parasitic ringing. Second, the comparatively lower gate threshold voltage could reduce noise margins. A third concern for these devices – although not very serious – is the higher gate-leakage current, which could increase gate-driver dissipation.

The depletion mode GaN device offers both performance as well as manufacturing advantages. Its normally "on" nature may be a problem during power-up and other abnormal operating conditions, however. It also requires the use of a negative supply. You can overcome this problem by connecting the depletion mode GaN high-electron mobility transistor (HEMT) in series with a low-voltage silicon MOSFET in the cascoded d-GaN structure. The gate of the HEMT is shorted to the source of the MOSFET, while the HEMT source connects to the drain of the MOSFET [1]. As **Figure 1** shows, the gate-to-source voltage of the HEMT is the source-to-drain voltage of

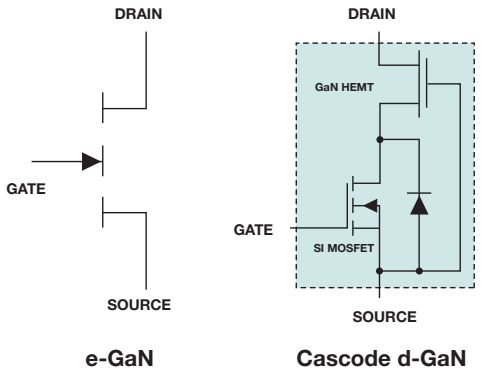

***Figure 1**. Symbols of e-GaN and cascode d-GaN devices highlight structural difference.*

the MOSFET. So the silicon MOSFET can control the turning on and off of the GaN HEMT.

The main advantage of this structure is that the complete cascoded d-GaN switch has the gate characteristics of a low-voltage silicon MOSFET. Therefore, existing commercial MOSFET gate drivers can easily drive the cascoded d-GaN switch. Also, because the gate characteristics of silicon MOSFETs are well-known, there are no unknowns to deal with.

You will have to make some compromises in overall performance because of the additional series silicon switch. The most significant impact on performance is arguably due to the reverse recovery associated with the body diode of the silicon MOSFET. Because the cascoded d-GaN switch is a series combination, it will have reverse recovery while conducting in a reverse direction, unlike an e-GaN switch. The next significant effect is the possibility of the silicon MOSFET avalanching during turn-off due to the charge imbalance between the drain-to-source capacitances of the two series devices. This can potentially increase switching losses and decrease reliability.

A cascoded d-GaN has increased packaging complexity and cost due to the additional series silicon switch. The higher number of devices and interconnections increase issues related to reliability. Parasitic inductance and capacitance between the Silicon switch and GaN HEMT may cause delay and oscillation during switching transients and impact electrical performance.

Another unfavorable effect with d-GaN devices is the increased on-resistance because of the addition of the on-resistance of the silicon MOSFET. The increase can be significant for lower-voltage (<200 V) cascoded d-GaN devices. So for low voltages, e-GaN switches are a better choice. For a high-voltage (600 V) cascoded d-GaN device, the additional resistance may be only about 5% of the overall on-resistance [2]; at this voltage level, cascoded d-GaN is still a viable option.

TI direct-drive GaN

After comparing e-GaN and d-GaN structures, it is obvious that most of the issues associated with the cascoded d-GaN are from the simultaneous switching of the silicon MOSFET and GaN HEMT. TI's direct-drive technology overcomes this problem by using only the silicon MOSFET to enable the device. **Figure 2** compares the configuration.

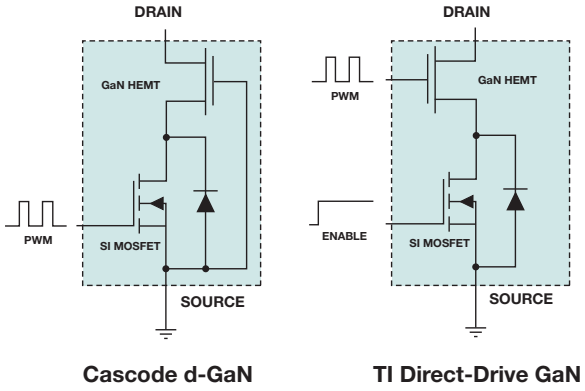

***Figure 2**. Configuration difference between cascode d-GaN and Direct-Drive GaN.*

As mentioned earlier, in cascode GaN, both the silicon and GaN devices turn on and off together. However, in the TI direct-drive GaN, the silicon MOSFET is only used to overcome the problem of power-up shoot-through. The silicon MOSFET is not switching; it turns on during power-up and stays on until power-down with an enable signal that's applied only when the negative bias voltage to turn off the GaN HEMT is available [3]. Integrating the negative voltage supply and gate drives along with the power switches ensures reliable and precise control over switching of both the silicon MOSFET and GaN HEMT. Driving the GaN gate directly reduces the gate charge significantly. And completely eliminating the body diode's reverse recovery and silicon-switch avalanching results in a considerable reduction in switching losses.

Other advantages resulting from the integration of the drive circuit into the power devices include the ability to control the switching slew rate, cycle-by-cycle over-current protection by sensing the voltage drop across the silicon MOSFET and over-temperature protection.

Device packaging

Because GaN devices are capable of very fast switching, the parasitics associated with the package are extremely important. In certain cases, they can severely limit the device performance.

Of all parasitic elements, common source inductance (CSI) is the most significant because of its effects on electrical performance. The overall CSI is the sum of the source inductance internal to the package and the lead inductance of the package itself. CSI has the potential to create ringing across the drain-to-source and gate-to-source voltages in the presence of high di/dt in the drain-to-source circuit, resulting in increased losses [4] and false switching [5]. In e-GaN devices, the ringing in VGS can even result in breakdown of the gate, as the safety margin is limited.

In silicon MOSFETs, a common practice is to damp this ringing by increasing the gate resistance and slowing down the switching. This isn't advisable for GaN devices because they will lose their inherent fast switching ability. Another solution is to provide a Kelvin source connection to remove CSI from the gate-drive circuit. While this can address the false switching problem, drain-to-source ringing can still be present. A through-hole package like TO-220 is not a very good option for GaN devices, as the significant lead inductances can prevent the optimal utilization of their fast switching capability. Also, the center drain arrangement of the TO-220 package is not ideal for the layout of a fast switching device. It would be better to use surface-mount device (SMD) packages with the Kelvin source pin close to the gate pin. Using devices that have the gate driver integrated with the GaN switch itself (as in TI's direct-drive devices) is even better as it can avoid problems with external layouts.

Thermal management is another package-related consideration. Most SMD packages depend on thermal transfer through the printed circuit board (PCB) for heatsinking. To improve thermal performance, the user guide of a TI GaN daughter-card explains how to attach the heatsink to the PCB [6]. Placing this below the thermal pad of the package reduces thermal resistance to the heatsink connected on the opposite side of the PCB. While the TO-220 package is better for thermal management because the metal tab is available for heatsinking, be aware of the issues discussed in this paper before considering its use.

Another package-related consideration is related to electromagnetic interference (EMI). Most switching power circuits have the drain as the switching node. But connecting the thermal pad to the drain can result in high common-mode and radiated EMI. Therefore, a source-connected thermal pad is a better choice from an EMI perspective.

In certain applications, the source can be the switching node. In such cases, connecting the heatsink (directly or through a capacitor) to a quiet node (DC bus positive or return) can help reduce EMI.

Drain voltage rating

By design, most practical GaN devices are not avalanche-capable. So a sufficient voltage rating is important. Take care to not exceed the breakdown voltage rating even during transient events. A voltage rating of 600 V is generally adequate at bus voltages of up to 480 V for buck, boost and bridge topologies (including half and full bridge, inductor-inductor capacitor [LLC], phase-shifted full bridge [PSFB], etc.).

Output capacitance

There are two different output-capacitance parameters for a switching power device: one is time-related and the other is energy-related. Time-related output capacitance, $C_{O(tr)}$, is more important in soft-switching topologies, as it determines the dead time required for zero voltage switching (ZVS). For GaN devices, this parameter is significantly lower (5x-10x) than silicon super-junction MOSFETs. You may also see this parameter specified in terms of charge (Q_{OSS}). In ZVS topologies, the reduced $C_{O(tr)}$ offers significant advantages compared to silicon MOSFETs because the reduced dead time results in lower circulating currents.

Although $C_{O(tr)}$ is significantly lower for GaN devices, the same is not true for energy-related output capacitance, $C_{O(er)}$. You may see the same parameter expressed in terms of energy (E_{OSS}). $C_{O(er)}$ is slightly higher for a cascoded d-GaN device but almost equal for an e-GaN device compared to a top-of-the-line silicon super-junction MOSFET because, while the output capacitance (C_{OSS}) of GaN devices does not vary much with voltage, it is very nonlinear for silicon super-junction MOSFETs. Since the capacitance is much higher for super-junction MOSFETs at lower voltages and lower at higher voltages, the energy content of the overall charge can be similar. However, as C_{OSS} is much more linear for GaN devices, the hysteresis associated with the energy stored in it is lower compared to a silicon super-junction MOSFET of comparable E_{OSS}, allowing much more of the energy to be recovered in a soft-switching application.

Gate charge

Gate charge is the parameter that indicates the device's ability to switch fast. The lower value of the sum $Q_{GS2} + Q_{GD}$ indicates the device's ability to achieve higher dV/dt – and consequently reduced switching losses. Typically, GaN devices have a significant advantage here. e-GaN devices have about 10x and d-GaN devices have about 2x-5x lower gate charges compared to silicon super-junction MOSFETs. You can also look at the R_{ON} x Q_G figure of merit to see if sufficiently low conduction losses accompany low switching losses.

dV/dt and di/dt sensitivity

CSI-related false switching due to high di/dt was previously referenced in the "Device packaging" section. Since the problem is mostly package and layout related, reducing CSI through proper package selection and proper layout is the solution to di/dt-related issues.

The dV/dt sensitivity of power-switching devices is caused by the interaction between the various parasitic capacitances and gate-drive circuit impedances. This is also true for GaN devices. **Figure 3** shows various parasitic capacitances and the currents through them during a positive-going dV/dt event across the drain source.

During a dV/dt event, the drain-source capacitance (C_{DS}) gets charged; at the same time, the gate-drain (C_{GD}) and gate-source (C_{GS}) capacitors also

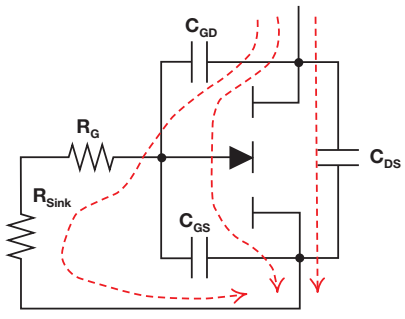

***Figure 3**. Parasitic capacitances and currents in a GaN power device.*

charge in series. If unaddressed, the charging current through the C_{GD} capacitor will flow through and charge C_{GS} beyond the gate threshold voltage (V_{TH}) and turn the device on. This event, sometimes called Miller turn-on and well-known in the context of MOSFET switching, can be very dissipative. To determine the dV/dt sensitivity of a power-switching device, you can use a figure of merit called the Miller charge ratio (Q_{GD}/Q_{GS1}). A Miller charge ratio of less than 1 will guarantee theoretical dV/dt immunity. It may not always be possible to get this ratio lower than 1, however, especially with higher voltage devices. In such cases, the effectiveness of diverting the C_{GD} capacitor charging current through the gate-driving circuit determines the dV/dt immunity of the circuit. Even though in **Figure 3** the gate-drive circuit shows only resistances, the drive circuit can involve inductance due to the layout, which can have a significant impact on the effectiveness of diverting the charging current. So the gate-drive circuit layout becomes a critical factor in improving dV/dt immunity. A co-packaged gate driver can have a significant positive impact due to the lower impedance gate driving that is possible through its use.

The gate-threshold voltage, V_{TH}, is also of great importance in ensuring dV/dt immunity. While a higher V_{TH} is preferable, the structure of the e-GaN switch results in lower gate-to-source voltage levels. Cascoded d-GaN devices are comparatively better than e-GaN devices, as the gate structure is silicon and the gate-to-source voltage levels are same as those of silicon MOSFETs.

Reverse conduction

The reverse conduction characteristics of the power-switching device are important in many switching topologies that use a totem-pole (half-bridge) power stage. While the forward drop of the body diode in a silicon MOSFET is low, ensuring low conduction losses, its reverse recovery is very slow, resulting in significantly high switching losses.

Even though GaN devices do not have a reverse body diode, they are capable of conducting in reverse direction, as they are inherently bidirectional devices. As soon as the reverse voltage across them exceeds the gate threshold voltage, they can start conducting. This conduction can resemble the effect of a reverse body diode, with a cut-in forward drop equal to the gate threshold voltage and dynamic resistance equal to the on-resistance. As this reverse conduction is a majority carrier effect, there is no associated reverse recovery. But since the gate threshold voltage is much higher than a junction diode forward voltage, the conduction losses can be significant. Therefore, in most applications that need reverse conduction, you may need careful dead-time-optimized synchronous rectification.

Cascoded d-GaN devices have reverse recovery because of the series-connected low-voltage silicon MOSFET, although the Q_{rr} is considerably lower than the reverse body diode of a comparable silicon super-junction MOSFET.

TI's direct-drive architecture completely eliminates the reverse recovery of the silicon MOSFET, as the channel is always on during switching and the diode never comes into operation. However, like in an e-GaN FET, you should address the higher voltage drop during reverse operation with a robust synchronous rectification scheme.

To soft switch or not

There is a general perception among many power system designers that GaN power switches can make soft or resonant switching topologies irrelevant due to their ability to switch very fast. The assumption is that fast switching capability can achieve comparable or even better efficiencies with

hard-switching topologies; thus, soft switching may become irrelevant. While this is true at the switching frequencies currently achievable with silicon MOSFETs, there is significant E_{OSS} loss associated with GaN devices, as discussed elsewhere in this paper. As the switching frequency increases, the E_{OSS} loss becomes the most significant loss component. Since the stored energy in the output capacitance of GaN devices is much more easily recoverable compared to silicon super-junction MOSFETs, it makes a lot of sense to go for soft or resonant switching, especially at multi-megahertz switching frequencies.

Conclusion

The device architecture, packaging and performance parameters of d-GaN and e-GaN devices continue to evolve towards as efficient, robust and cost-effective alternatives to silicon MOSFETs in power conversion. No doubt, many of the performance parameters discussed in this whitepaper will be improved significantly in the future. Higher levels of integration of GaN devices like half bridge devices and integrated gate driver with protection circuits will make their usage in power conversion far easier. The adoption of GaN devices in soft switching topologies can push the power density of power converters to levels unprecedented with silicon switching technology.

References

1. W. Liu, H. Zhou and E. Persson. “Switching Characteristics of Cascode GaN Switches,” PCIM Europe, 2015.
2. A. Lidow, M. de Rooij, J. Strydom and D. Reusch. “GaN Transistors for Efficient Power Conversion,” Efficient Power Conversion Corp., APEC 2013 Educational Seminar S7, p. 16.
3. P. Brohlin, Y.K. Ramadass and C. Kaya. “Direct-drive configuration for GaN devices,” Texas Instruments white paper (SLPY008), October 2016.
4. D. Jauregui, B. Wang and R. Chen. “Power Loss Calculation with Common Source Inductance Consideration for Synchronous Buck Converters,” Texas Instruments application report (SLPA009A), July 2011.
5. J. Wang and H. Shu-Hung Chung. “Impact of Parasitic Elements on the Spurious Triggering Pulse in Synchronous Buck Converter,” IEEE Transactions on Power Electronics, Vol. 29, Issue 12, December 2014, p. 6672-6685.
6. “Using the LMG3410-HB-EVM Half-Bridge and LMG34XXBB-EVM Breakout Board EVM,” Texas Instruments user’s guide (SNOU140A), May 2017.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265